Logic design A

Finalità
The course objective is to introduce the basic techniques for analysis and design of synchronous digital systems. Both traditional methodologies and algorithmic techniques exploited in industrial Design Automation flows are presented.

Programma
Introduction to digital systems
Evolution of electronic technologies. Objectives and limitations of synchronous digital systems.

Combinational logic design
1 - Review: Canonical and general logic expressions (SP and PS). Analysis and synthesis of fully specified logic functions based on Karnaugh maps.
2 - Other two-level logic analysis and synthesis techniques: Incompletely specified logic functions. Multiple output circuits (multiple prime implicants/implicates method). Analysis and synthesis of NAND and NOR circuits.
3 - CAD tools for combinational network design: Quine-McCluskey algorithm. Espresso. Logic simulation.
4 - Multilevel logic and integrated circuit-based design: Expression factorization and decomposition. Combinational logic design based on standard MSI and LSI parts (Multiplexers, Decoders, Encoders, ROMs, AOI components).
5 - Programmable logic (PLA, PAL, GAL).
6 - Dedicated combinational circuits: Arithmetic circuits (adders, comparators, ALU). Transocoders. Parity and Hamming circuitry. XOR based circuits.
7 - Transient phenomena in combinational circuits: static and dynamic hazards.

Synchronous sequential logic design
1 - Mealy and Moore machines. Elementary logic circuits with delays and feedback. Fundamental mode operation.
2 - Basic memory elements: SR and D Latches; D, JK, and T Flip-Flops. Timing issues. Timing in synchronous circuits.
3 - Finite state automata: Automata description techniques (state diagrams, flow tables, description languages). State minimization.
4. Analysis and synthesis of synchronous sequential circuits: State encoding. State memory implementation with Flip-Flops and Latches.
5 - The synchronous/asynchronous interface: Flip-Flops with Preset and Clear commands. Management of asynchronous and pulsed inputs in synchronous circuits.
6 - Counters and Registers: Design of binary counters, Johnson counters, counters with arbitrary state encoding. Parallel registers and shift registers.
7 - Sequential programmable logic (FPGA).

Analysis and synthesis of complex digital systems
1 - Sequential circuit design based on standard integrated circuits (registers, counters, shift-registers, sequencers, MUXes, etc.).
2 - Complex circuit design by decomposition in datapath and control unit.
3 - Design techniques for pipelined circuits.
4 - Hardware description languages.

Attività d'esercitazione
Guided exercise solution in classroom will be routinely performed. In addition, laboratory sessions involving simple CAD tools for logic design entry and digital simulation are planned.

Modalità d'esame
The recommended exam modality is to undertake the two planned mid-term written tests during the teaching period. Alternatively, a single written test covering the whole course program must be passed in any of the scheduled official exam dates. Tests include both theory questions and design exercises.

Propedeuticità
Fondamenti di informatica B.

Testi consigliati
Lecture notes from the instructor (available from the course web site).
M.M. Mano, Digital Design, 3/e, Prentice Hall, 2002.
The following textbook, already available to most students, covers only part of the course syllabus:
M.M. Mano, C. R. Kime, Reti Logiche, Addison-Wesley/Pearson Education Italia, 2002.